TIMER LOCKOUT CIRCUIT FOR SYNCHRONOUS APPLICATIONS

Abstract

A SDRAM including: at least one bank of DRAM cells; the SDRAM operable to a first specification defined by a first clock frequency, a first write recovery time and a first time interval for precharge to row address strobe; and means for programming the SDRAM operable to a second specification defined by a second clock frequency, a second write recovery time and a second time interval for precharge to row address strobe.